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EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/028,298	GOLDBERG ET AL.	
	Examiner	Art Unit	
	CHUONG T. HO	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-17 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17,19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 12/11/07 have been entered and made of record.

2. Applicant's arguments with respect to claims 1, 3-9, 11-17 and 19-24 have been considered but are moot in view of the new ground(s) of rejection.

3. Claims 1, 3-9, 11-17 and 19-24 remain pending.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/11/07 has been entered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-9, 11-17, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takebe (Patent Number: 5,357,517) in view of Kularatna et al. (Patent No.: US 6,904,034 B2).

Regarding to claim 1, Takebe discloses when errors frequently take place at a plurality of different locations, issuance of the operation's instruction causes the error display contents to be held (col. 4, lines 55-56); comprising:

- Realizing data error during communication (col. 5, lines 25-28, when such a data frame signal containing the actuator control data DO as shown in FIG. 5(a) is sent from the main controller 100 to the node 10-1, the data frame signal is sequentially propagated from the node 10-1 via the nodes 10-2, 10-3, 10-4 and to the node 10-5, which results in that the actuator control data DO in the data frame signal are allocated to the corresponding nodes and at the same time the detection data of the sensor group obtained at the respective nodes are taken into the data frame signal);
- Providing an error indicator at said link when said data error is detected (col. 5, lines 35-45, An error detecting circuit 35 receives the bit Ea in an error signal ERR (refer to FIG. 6) attached to the end of the data frame signal and indicative of the presence or absence of an error and a code CRC in the data frame signal, judges "1" or "0" in the bit Ea to detect the presence or absence of an error. And the error detecting circuit 35, when the bit Ea is "0", detects the error in the data frame signal through CRC check. When detecting the error in this way, the error detecting circuit 35 inputs a detection signal ED to an error counter 40 and an

update enabling signal generating circuit 65. The error counter 40 counts the received detection signal ED and outputs a counted value to the CPU 30).

- Providing a clear indicator at said link when said data error is resolved (col. 6, lines 15-30, The clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the command received from the CPU 30 and in puts the signal CLR2 to these registers) (col. 6, lines 40-42, the error kind and position registers 45 and 50 can be updated. More specifically, in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared).

However, Takebe is silent to disclosing utilizing a blocking agent at said link to block between said at least two communicating nodes in response to said error indicator.

Kularatna discloses error detection, recovery procedures, notification of unrecoverable errors (col. 4, line 55); comprising:

- Utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission (see col. 5,

lines 42-45, network service control provides blocking procedure used by NSE to inform a peer NSE when an NS-VC becomes unavailable for data transmission. An unblocking procedure is used to remove the blocking restriction after the NS-VC become available); utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes.

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to utilize a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilize said blocking agent to unblock said blocked communication between said at least two communication nodes in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

Regarding to claim 9, Takebe discloses when errors frequently take place at a plurality of different locations, issuance of the operation's instruction causes the error display contents to be held (col. 4, lines 55-56); comprising:

- Realizing data error during communication (col. 5, lines 25-28, when such a data frame signal containing the actuator control data DO as shown in FIG. 5(a) is sent from the main controller 100 to the node 10-1, the data frame signal is sequentially propagated from the node 10-1 via the nodes 10-2, 10-3, 10-4 and to the node 10-5, which results in that the actuator control data DO in the data frame signal are allocated to the corresponding nodes and at the same time the detection data of the sensor group obtained at the respective nodes are taken into the data frame signal);
- Providing an error indicator at said link when said data error is detected (col. 5, lines 35-45, An error detecting circuit 35 receives the bit Ea in an error signal ERR (refer to FIG. 6) attached to the end of the data frame signal and indicative of the presence or absence of an error and a code CRC in the data frame signal, judges "1" or "0" in the bit Ea to detect the presence or absence of an error. And the error detecting circuit 35, when the bit Ea is "0", detects the error in the data frame signal through CRC check. When detecting the error in this way, the error detecting circuit 35 inputs a detection signal ED to an error counter 40 and an update enabling signal generating circuit 65. The error counter 40 counts the received detection signal ED and outputs a counted value to the CPU 30).
- Providing a clear indicator at said link when said data error is resolved (col. 6, lines 15-30, The clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating

part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the command received from the CPU 30 and in puts the signal CLR2 to these registers) (col. 6, lines 40-42, the error kind and position registers 45 and 50 can be updated. More specifically, in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared).

However, Takebe is silent to disclosing utilizing a blocking agent at said link to block between said at least two communicating nodes in response to said error indicator.

Kularatna discloses error detection, recovery procedures, notification of unrecoverable errors (col. 4, line 55); comprising:

- Utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission (see col. 5, lines 42-45, network service control provides blocking procedure used by NSE to inform a peer NSE when an NS-VC becomes unavailable for data transmission. An unblocking procedure is used to remove the blocking restriction after the NS-VC become available); utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes.

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to utilize a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilize said blocking agent to unblock said blocked communication between said at least two communication nodes in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

7. Regarding to claim 17, Takebe discloses when errors frequently take place at a plurality of different locations, issuance of the operation's instruction causes the error display contents to be held (col. 4, lines 55-56); comprising:

- A communication interconnect (figure 1, figure 4);
- A optional display device (figure 1, main controller 100, display device 85) coupled to said communication interconnection;
- A memory unit (figure 1, error-kind register 45) coupled to said communication interconnect, said processor (figure 1, CPU 30) for executing a system of error protection in a network environment;

- Realizing data error during communication (col. 5, lines 25-28, when such a data frame signal containing the actuator control data DO as shown in FIG. 5(a) is sent from the main controller 100 to the node 10-1, the data frame signal is sequentially propagated from the node 10-1 via the nodes 10-2, 10-3, 10-4 and to the node 10-5, which results in that the actuator control data DO in the data frame signal are allocated to the corresponding nodes and at the same time the detection data of the sensor group obtained at the respective nodes are taken into the data frame signal);
- Providing an error indicator at said link when said data error is detected (col. 5, lines 35-45, An error detecting circuit 35 receives the bit Ea in an error signal ERR (refer to FIG. 6) attached to the end of the data frame signal and indicative of the presence or absence of an error and a code CRC in the data frame signal, judges "1" or "0" in the bit Ea to detect the presence or absence of an error. And the error detecting circuit 35, when the bit Ea is "0", detects the error in the data frame signal through CRC check. When detecting the error in this way, the error detecting circuit 35 inputs a detection signal ED to an error counter 40 and an update enabling signal generating circuit 65. The error counter 40 counts the received detection signal ED and outputs a counted value to the CPU 30).
- Providing a clear indicator at said link when said data error is resolved (col. 6, lines 15-30, The clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating

part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the command received from the CPU 30 and in puts the signal CLR2 to these registers) (col. 6, lines 40-42, the error kind and position registers 45 and 50 can be updated. More specifically, in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared).

However, Takebe is silent to disclosing utilizing a blocking agent at said link to block between said at least two communicating nodes in response to said error indicator.

Kularatna discloses error detection, recovery procedures, notification of unrecoverable errors (col. 4, line 55); comprising:

- Utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission (see col. 5, lines 42-45, network service control provides blocking procedure used by NSE to inform a peer NSE when an NS-VC becomes unavailable for data transmission. An unblocking procedure is used to remove the blocking restriction after the NS-VC become available); utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes.

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to utilize a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission and utilize said blocking agent to unblock said blocked communication between said at least two communication nodes in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

8. Regarding to claim 3, Takebe discloses utilizing an error bit as said error indicator (col. 5, lines 35-36, indicative of the presence or absence of an error and a code CRC in the data frame signal judges "1" or "0" in the it Ea to dtect the presence of absence of an error).

9. Regarding to claim 4, Takebe discloses the limitations of claim 3 above.

However, Takebe is silent to disclosing utilizing a link barrier as said blocking agent to provide said blocking of said communication between said at least two communicating nodes.

Kularatna discloses utilizing a link barrier (col. 5, lines 43-45, Network service control) as said blocking agent to provide said blocking of said communication between said at least two communicating nodes.

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes utilizing a link barrier as said blocking agent to provide said blocking of said communication between said at least two communicating nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to utilize a link barrier as said blocking agent to provide said blocking of said communication between said at least two communicating nodes.in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

10. Regarding to claim 5, Takebe discloses generating said clear indicator at each of said at least two communicating nodes; and providing said clearing indicator to said link from each of said at least two communication nodes (col. 6, lines 15-30, The clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the command received from the CPU 30 and in puts the signal CLR2 to these registers) (col. 6, lines 40-42, the error kind and position registers 45 and 50 can be

updated. More specifically, in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared).

However, Takebe is silent to disclosing resolving said data error at each of said at least two communication nodes.

Kularatna discloses resolving said data error (col. 5, lines 43-47, by unblocking the block when the transmission is available) at each of said at least two communication nodes.

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes resolving said data error at each of said at least two communication nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to resolve resolving said data error at each of said at least two communication nodes .in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

11. Regarding to claim 6, Takebe discloses generating multiple clearing indicators by said at least two communication nodes, wherein each of said at least two communication nodes generates one of said multiple clear indicators (col. 6, lines 15-20, the error kind register) subsequent to its said resolving of said error, wherein each of said clear indicators corresponds to an associated corresponding position relative to

said at least two communication nodes (col. 5, lines 48-50, error position register), and wherein each of said clearing indicators (col. 6, lines 15-20).

However, Takebe is silent to disclosing resets a link usage indicator set by each of said at least two communicating nodes.

Kularatna discloses resets (figure 2, reset) a link usage indicator set by each of said at least two communicating nodes (col. 5, lines 43-45).

Both Takebe and Kularatna disclose the error detection. Kularatna recognizes resets a link usage indicator set by each of said at least two communicating nodes. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system Takebe with the teaching of Kularatna to reset a link usage indicator set by each of said at least two communicating nodes .in order to provide error display (Takebe, col. 4, lines 10-11). Therefore, the combined system would have been enable to provide the routing and control information necessary to allow two system component to communicate (Kularatna, col. 1, lines 56-57).

12. Regarding to claim 7, Takebe discloses wherein a first storage (col. 5, lines 47-50, error kind register 45) and second storage element are disposed (col. 6, lines 15-20, the clear signal generating part 70 generates a clear signal) at said link, said first storage element and said second storage element for maintaining a real time error status of said at least two communicating nodes (col. 5, lines 38-40, the error kind register 45 and position register 50).

13. Regarding to claim 8, Takebe discloses wherein first storage element (figure 1, col. 5, lines 46-50, error kind register 45) and a second storage element (clear signal

generating part 70) are disposed at each of said nodes, said first storage element (error kind register 45) and said second storage element (clear signal generating part 70) for maintaining a real-time error status of said at least two communicating nodes (col. 5, lines 38-40, the error kink register 45 and position register 50).

14. Regarding to claim 11, claim 11 is rejected the same reasons of claim 3 above.

15. Regarding to claim 12, claim 12 is rejected the same reasons of claim 4 above.

16. Regarding to claim 13, claim 13 is rejected the same reasons of claim 5 above.

17. Regarding to claim 14, claim 14 is rejected the same reasons of claim 6 above.

18. Regarding to claim 15, claim 15 is rejected the same reasons of claim 7 above.

19. Regarding to claim 16, claim 16 is rejected the same reasons of claim 8 above.

20. Regarding to claim 19, claim 19 is rejected the same reasons of claim 3 above.

21. Regarding to claim 20, claim 20 is rejected the same reasons of claim 4 above.

22. Regarding to claim 21, claim 21 is rejected the same reasons of claim 5 above.

23. Regarding to claim 22, claim 22 is rejected the same reasons of claim 6 above.

24. Regarding to claim 23, claim 23 is rejected the same reasons of claim 7 above.

25. Regarding to claim 24, claim 24 is rejected the same reasons of claim 8 above.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gross et al. (Patent No.: US 6,742,146 B2); Karpuszka et al. (Patent No.: US 6,701,480 B1; Nakano (Pub.No.: US 2002/0040449 A1; Karpuszka (Pub.No.: US 2004/0237022 A1).

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ORGAD EDAN can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/08/08

HO, CHUONG
02/17/08